Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs

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***Abstract* —** We present the first **s**ub-10 nm diameter vertical nanowire transistors of any kind in any semiconductor system. These devices are InGaAs MOSFETs fabricated by a top-down approach using reactive ion etching, alcohol-based digital etch and Ni alloyed contacts. A record I_{on} of 350 μA/μm at I_{off} = 100 nA/μm and V_{dd} = 0.5 V is obtained in a 7 nm diameter device. The same device exhibits a peak transconductance ($g_{m,pk}$) of 1.7 mS/μm and minimal subthreshold swing (S) of 90 mV/dec at V_{ds} = 0.5 V, achieving the highest quality factor (defined as the ratio $g_{m,pk}$/S) of 19 reported in vertical nanowire transistors. Excellent scaling behavior is observed with $g_{m,pk}$ and I_{on} increasing as the diameter is shrunk down to 7 nm.

I. Introduction

The III-V vertical nanowire (VNW) MOSFET has emerged as a promising candidate for CMOS technology beyond the 10 nm node [1]. This device architecture combines the superior transport properties of III-V semiconductors [2] with the ultimate scalability of a vertical nanowire channel [3] where gate length, spacer thickness and contact length do not contribute to the footprint of the device [4]. InGaAs vertical nanowire MOSFETs have been demonstrated by bottom-up [5, 6] and top-down approaches [7-9]. Recently, remarkable improvement in device performance has been achieved using a bottom-up technique [5]. However, VNW MOSFETs with sub-10 nm diameter, demanded by future ultra-scaled logic applications [4], remain elusive. This is because of the difficulty of obtaining VNWs with small diameter and high aspect ratio [10] and the challenge to contact such narrow NWs. To date, the narrowest VNW transistor that has been claimed is a tunnel FET with a diameter of 11 nm, but no electrical characteristics were shown [11].

In this work, we exploit a new solvent-based digital etch (DE) technique [10] to achieve InGaAs VNWs down to 7 nm in diameter, the design point for a future 5 nm technology node [4]. The use of alloyed Ni has allowed us to create contacts in such a small diameter device. The resulting devices achieve record performance and represent the first sub-10 nm vertical nanowire transistor of any kind in any material system.

II. Process Technology

Fig. 1 shows the schematic device cross-section and heterostructure of our VNW MOSFETs. The starting heterostructure consists of an 80 nm undoped $In_{0.53}Ga_{0.47}As$ channel sandwiched between two n^+-contact regions. The top contact region features a highly-doped composite cap that comprises of (from top) 11 nm $In_{0.53}Ga_{0.47}As$/ 2 nm InAs/ 6 nm $In_{0.7}Ga_{0.3}As$ (n^+-doped with Te at a level of 7×10^{19} cm^{-3}) on top of 55 nm $In_{0.53}Ga_{0.47}As$ (n^+-doped with Si at 2×10^{19} cm^{-3}). The insertion of InAs/ $In_{0.7}Ga_{0.3}As$ layers was intended to reduce the contact resistance as InGaAs forms better ohmic contacts when the InAs composition is high [12]. The top 11 nm $In_{0.53}Ga_{0.47}As$ was designed to be sacrificed during the process to reveal layers with higher InAs concentration underneath.

Device fabrication followed our previous work [9, 10] (process flow outlined in Fig. 2) but incorporated a number of innovations to reach sub-10 nm VNW transistors. Water-based DE [13], although capable of precision dimension engineering and also successful in mitigating surface damage introduced during dry etch, results in device destruction when attempting to cross below 10 nm in diameter (D) [10]. Nanowire breakage takes place due to the high surface tension of water-based acid used in the oxide removal step. Fig. 3 (a) [10] shows an arsenide VNW array (initial diameter = 22 nm) after 7 cycles of water-based DE. A final NW diameter of 8 nm is expected but all structures are destroyed. In contrast, Fig. 3 (b) [10] shows an identical sample processed side-by-side etched in 10% H_2SO_4:methanol, with a yield of 90% in VNWs with 5.5 nm diameter. Fig. 4 shows a 30 nm InGaAs VNW right after dry etch (left), then reduced to D = 7 nm after 10 cycles of DE in 10% H_2SO_4:methanol (right) used for device fabrication. A vertical sidewall is obtained towards the top of the NW where the active device layers are.

Another challenge to obtain functional sub-10 nm VNW devices is contacting the tiny NW top. For non-alloyed contact metal such as Mo or W, a mushroom-shaped stop contact [5, 13] is necessary to create a wider NW tip and avoid full depletion under the contact. This top heavy approach makes the structure mechanically fragile and adds considerable process complexity. In this work, in addition to Mo, Ni alloyed contacts were investigated since Ni reacts with InGaAs to form highly conducting NiInGaAs. The electrical performance of devices with Mo and Ni contacts, each with 30 nm thickness, was compared. In order to improve the device contact and oxide/semiconductor interface, a final rapid thermal annealing in N_2 (referred as RTA) or forming gas (referred as FGA) at 200 – 350ºC for 1 min was introduced after the completion of device fabrication. Sequential annealing experiments were performed to optimize the annealing conditions.

The final transistors feature a single NW with a channel length of 80 nm (the intrinsic InGaAs layer thickness), D = 7, 11, 15, 18, 30 or 40 nm and 2.5 nm Al_2O_3 gate oxide (EOT of

1.25 nm).

III. Electrical Characterization

Subthreshold, g_m and output characteristics (measured with bottom electrode as the source) of an exemplary D = 7 nm single NW device with Ni contact and FGA at 200°C are shown in Fig. 5. An ON/OFF ratio close to 10^5 is demonstrated at V_{ds} = 0.5 V. The minimum linear (V_{ds} = 0.05 V) and saturated (V_{ds} = 0.5 V) subthreshold swing (S_{lin} and S_{sat}) are 85 and 90 mV/dec, respectively, while DIBL is 222 mV/V. A record peak transconductance ($g_{m,pk}$) of 1.7 mS/μm is achieved with an ON resistance of 1100 Ω·μm. All figures of merit are normalized by the NW periphery.

Final annealing has a profound effect on the electrical characteristics of devices with Ni contact, especially for small diameters. The green data in the subthreshold and g_m characteristics in Fig. 5 show device behavior before FGA at 200°C, exhibiting 5 orders of magnitude less ON current and absence of gate control.

The output characteristics of Fig. 5 do not show current saturation, indicating that the top contact is still slightly Schottky and absorbs a significant fraction of V_{ds}. Considerable device variability is observed and the variation in the alignment of the gate metal edge to the top n^+ contact region as a result of planarization and etch back step is expected to be a significantly contribution. D = 7 nm devices that exhibit current saturation generally have less current. Fig. 6 shows the output characteristics of another D = 7 nm device that shows better saturation behavior.

Electrical characteristics of a D = 30 nm device with Mo contact after 300°C RTA are summarized in Fig. 7. S_{lin} and S_{sat} are 66 and 85 mV/dec, respectively and DIBL is 66 mV/V. The close to ideal linear subthreshold swing reveals that alcohol-based DE yields an excellent oxide/semiconductor interface after RTA. A $g_{m,pk}$ of 600 μS/μm is observed with R_{on} =1358 Ω·μm. The output characteristics show good current saturation.

IV. Diameter Scaling

The smallest diameter for functional devices with Mo contacts was found to be 15 nm, while many working D = 7 nm Ni-contacted transistors were obtained. Fig. 8 summarizes the key device figures of merit (FOMs) as a function of diameter for Ni and Mo devices under optimized final annealing conditions (200°C FGA for Ni and 300°C RTA for Mo). Each data point represent the mean value of 3 devices with the highest $g_{m,pk}$.

For Mo, R_{on} increases when the diameter is scaled and consequently $g_{m,pk}$ drops. Devices with D = 18 nm and below show weaker current saturation compared to wider devices. The subthreshold characteristics keep sharpening as the diameter is reduced. I_{on} reaches a peak at D = 30 nm due to the trade-off between electrostatics and contact resistance. Ni devices show dramatic improvement in $g_{m,pk}$ despite slightly rising R_{on} as the diameter scales down. This might be partially attributed to improved intrinsic g_m due to volume inversion [14]. Subthreshold swing also improves as D shrinks. As a consequence, I_{on} at a fixed I_{off} = 100 nA/μm and V_{dd} = 0.5 V increases down to D = 7 nm. With diameter scaling, DIBL in both kinds of devices first improves as expected, but then worsens, consistent with less current saturation in the output characteristics in devices with smaller diameter. This deterioration is likely due to the top contact becoming more Schottky. V_t at V_{ds} = 0.05 V was extracted at constant drain current of 1 μA/μm. In both devices V_t shifts positively as diameter scales, as expected.

To summarize, optimized Mo contact gives rise to better subthreshold characteristics because it supports annealing at higher temperature. Ni contacts, on the other hand, scale better and yield better contact resistance and overall device performance, with concerns about thermal stability and output saturation.

V. Benchmark

Fig. 9 benchmarks transport and electrostatics metrics in recently published InGaAs VNW MOSFETs by plotting $g_{m,pk}$ vs. minimum S_{sat}, both at V_{ds} = 0.5 V. This graph captures the trade-off that often exists between transport and electrostatics in MOSFETs. Our result for D = 7 nm device with Ni contact shows record g_m, highest quality factor of 19 and record I_{on}= 350 μA/μm at I_{off} = 100 nA/μm and V_{dd} = 0.5 V. This highlights the potential of the top-down VNW approach.

Fig. 10 benchmarks $g_{m,pk}$ in InGaAs and Si/Ge VNW MOSFETs as a function of nanowire diameter. With Ni-contacted transistors, we have broken through the 10 nm diameter boundary and entered the territory relevant for future ultra-scale logic applications. A remarkable result, is that the performance of these devices continues to improve as D shrinks with a record g_m achieved at D=7 nm.

VI. Conclusions

We demonstrate for the first time InGaAs VNW MOSFETs with sub-10 nm diameter. Record I_{on} and $g_{m,pk}$ are achieved in D = 7 nm devices with Ni contact. This is the first demonstration of VNW transistors of any kind in any semiconductor system with D < 10 nm.

Acknowledgment

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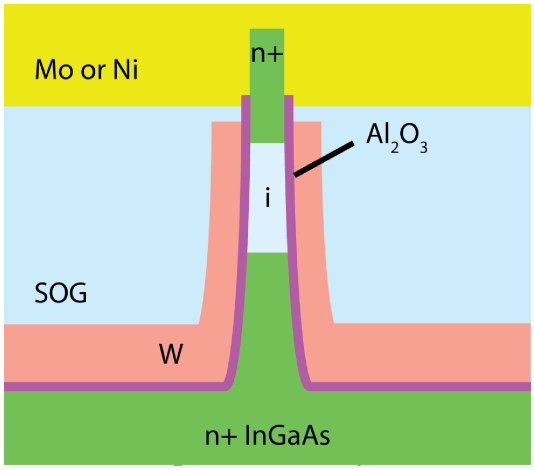
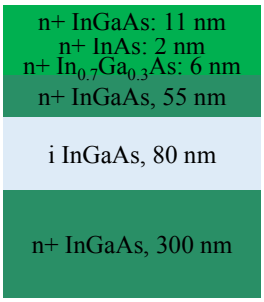


Starting heterostructure:



D = 40, 30, 18, 15, 11, 7 nm
No. of wires = 1
L_{ch} = 80 nm
EOT = 1.25 nm

Fig. 1. Schematics of the device cross-section, starting heterostructure and design parameters.

- HSQ mask definition by EBL
- Nanowire formation by dry etch
- Digital etch by H_2SO_4 in methanol & oxygen plasma.
- ALD 2.5 nm Al_2O_3 gate dielectric
- Sputter 40 nm W gate metal, followed by gate metal patterning
- 30 min forming gas annealing at 350°C
- Gate/top electrodes isolation by planarization and etch back (2 times)
- Contact via opening by dry etch
- Al_2O_3 removal in TMAH
- Sputter Mo or Ni as contact metal and S/G/D pad formation
- Rapid thermal annealing for 1 min

Fig. 2. Process flow for InGaAs VNW transistors by a top-down approach.

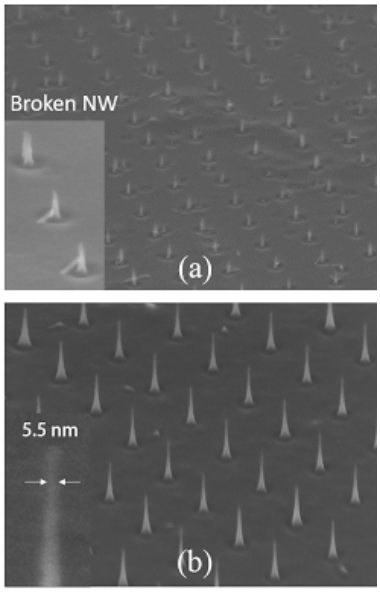


Fig. 3. InGaAs VNW array [10] after 7 DE cycles in (a) 10 % HCl in water and (b) 10 % H_2SO_4 in methanol. The nanowire yield in (a) is 0% while that in (b) is 90%. The insets show close ups of the etched structures.

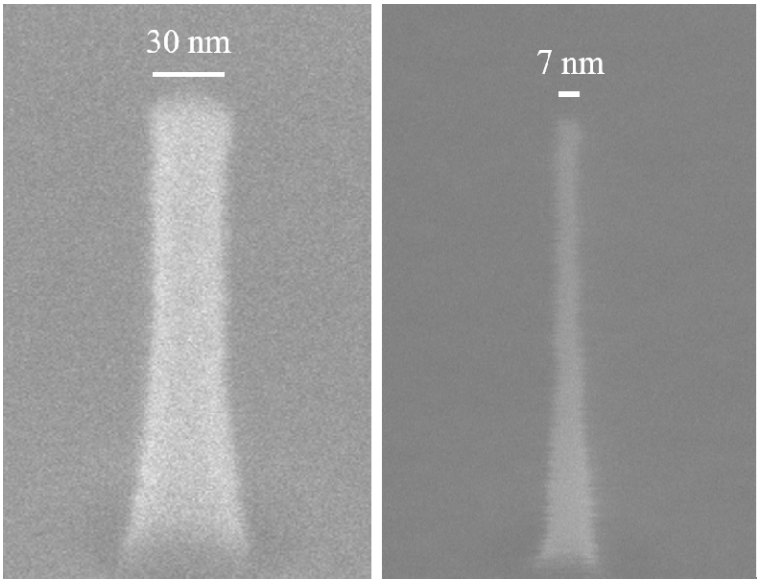


Fig. 4. D = 30 nm InGaAs nanowire (left) reduced to D = 7 nm (right) after 10 cycles of digital etch with 10 % H_2SO_4 in methanol.

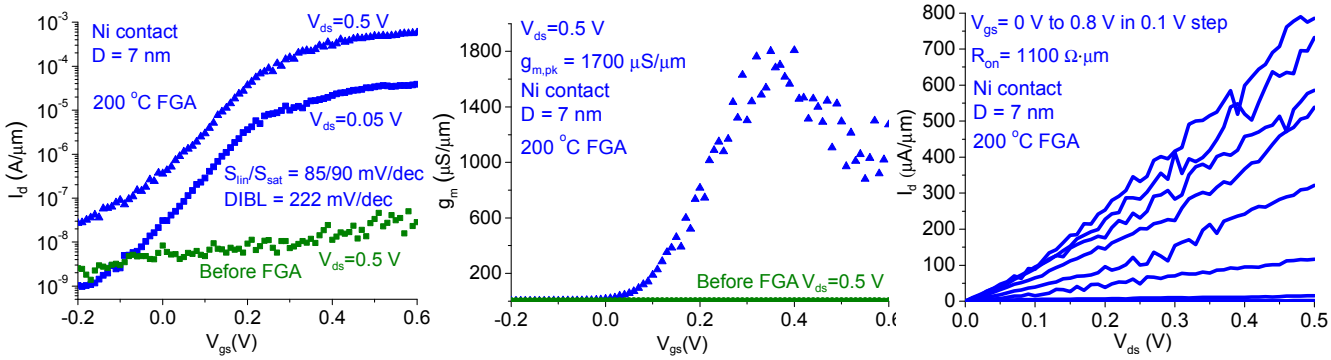


Fig. 5. Subthreshold, transconductance and output characteristics of an exemplar D = 7 nm InGaAs VNW MOSFET with Ni contact metal after 200°C FGA for 1 min. The green curves in the left and middle figures correspond to the device characteristics before RTA.

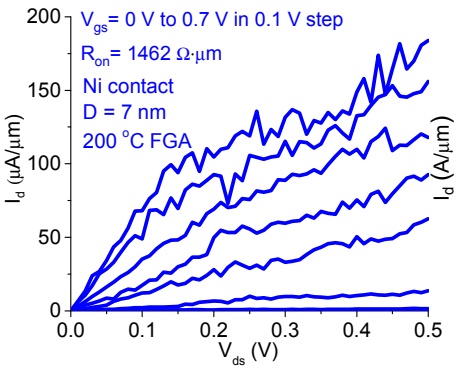


Fig. 6. Output characteristics of another D = 7 nm device with Ni contact that show better current saturation.

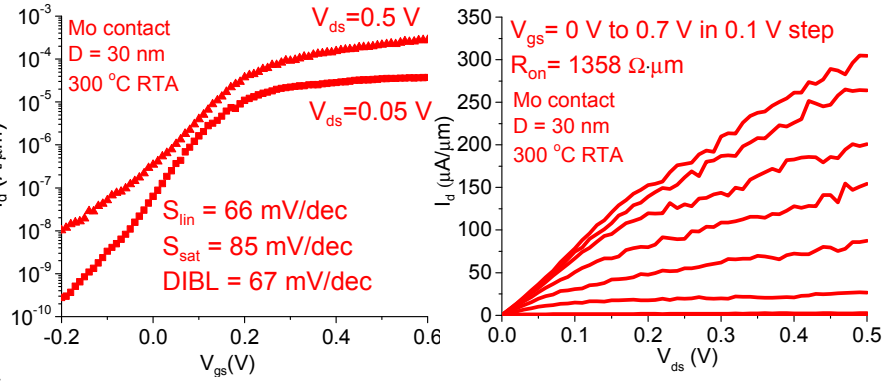


Fig. 7. Subthreshold and output characteristics of an exemplar D = 30 nm InGaAs VNW MOSFET with Mo contact metal after 300°C RTA in N_2 ambient for 1 min. The device shows close-to-ideal linear subthreshold swing of 66 mV/dec.

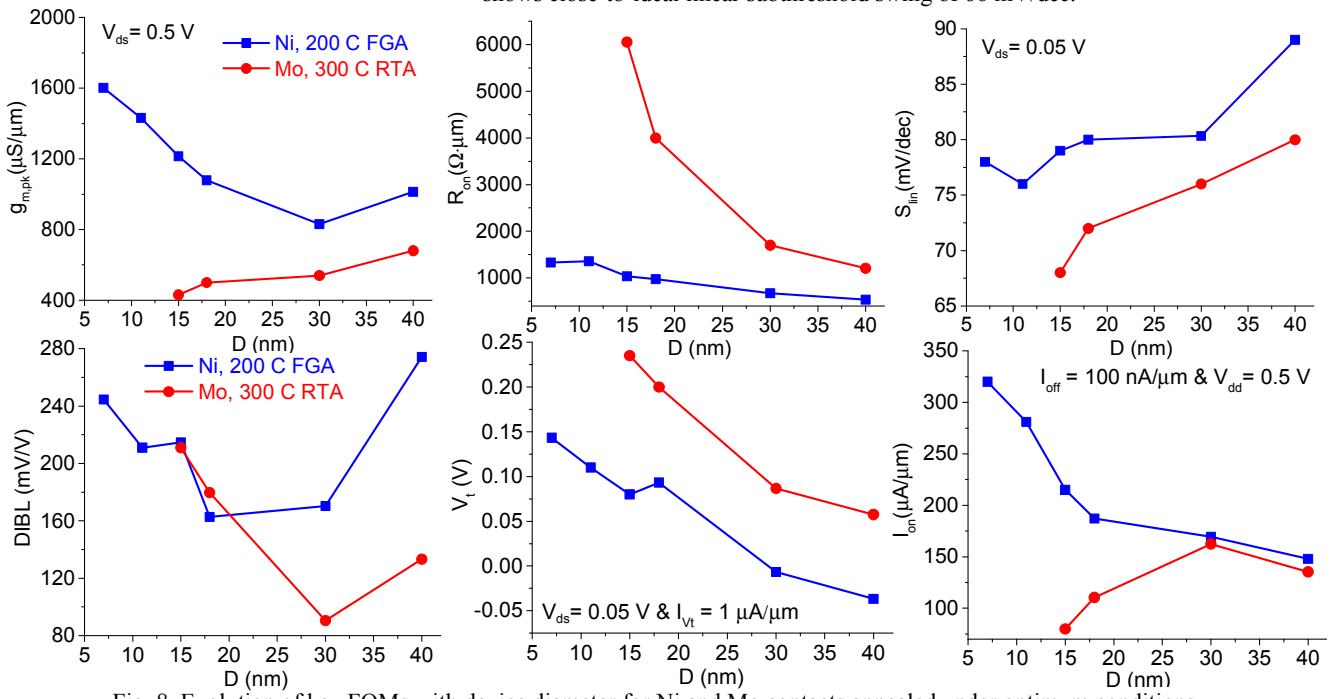


Fig. 8. Evolution of key FOMs with device diameter for Ni and Mo contacts annealed under optimum conditions.

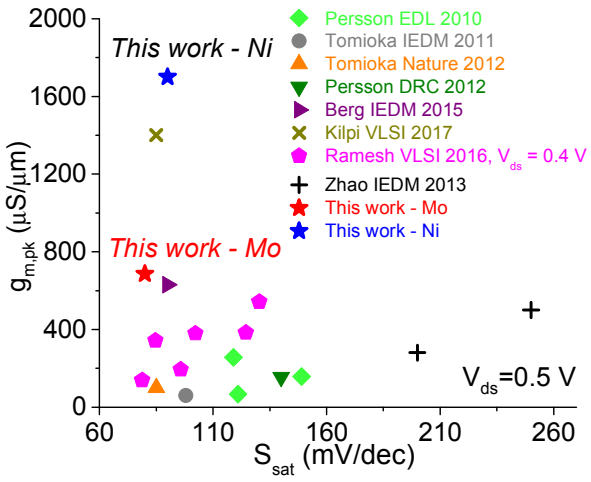


Fig. 9. Benchmark: $g_{m,pk}$ vs. minimum S_{sat} at V_{ds} = 0.5 V for InGaAs-based VNW MOSFETs. Our devices achieve the best balance between electrostatics and ON performance.

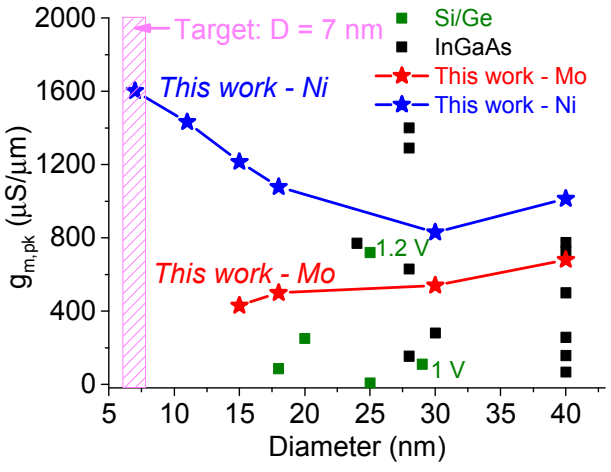


Fig. 10. Benchmark: $g_{m,pk}$ at V_{ds} = 0.5 V for InGaAs and Si/Ge VNW MOSFETs as a function of NW diameter. This work demonstrates the first sub-10 nm diameter VNW transistors and record $g_{m,pk}$.